WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising testmode circuitry adapted to maintain a pair of bitlines coupled to a memory cell within the device to the same logic state, wherein the bitlines are not maintained at the logic state during ordinary operation of the device.

2. The semiconductor memory device as recited in claim 1, further comprising a direct current from a voltage source to each of the pair of bitlines during operation of the testmode circuitry.

3. The semiconductor memory device as recited in claim 2, further comprising a user-determined voltage from the voltage source.

4. The semiconductor memory device as recited in claim 2, wherein the direct currents flow for a user-determined time.

5. The semiconductor memory device as recited in claim 2, wherein a path of each direct current comprises a respective local interconnect structure.

6. The semiconductor memory device as recited in claim 5, wherein each of the local interconnect structures comprises at least one contact through which the respective direct current passes when the bitlines are at the same logic state.

7. The semiconductor memory device as recited in claim 1, wherein the testmode circuitry is further adapted to force the pair of bitlines to circuit ground.

8. The semiconductor memory device as recited in claim 1, wherein the testmode circuitry is further adapted to hold the bitlines at the same logic state for a user-determined length of time.

9. A system for testing a semiconductor memory device, said system comprising testmode circuitry adapted to maintain a pair of bitlines coupled to a memory cell within the memory device to the same logic state, wherein the bitlines are not maintained at the logic state during ordinary operation of the device.

10. The system as recited in claim 9, wherein the testmode circuitry is adapted to force the pair of bitlines to a circuit ground potential.

11. The system as recited in claim 9, wherein the testmode circuitry is further adapted to maintain the pair of bitlines at the same logic state for a user-determined length of time.

12. The system as recited in claim 9, wherein the testmode circuitry is within the semiconductor memory device.

13. The system as recited in claim 9, wherein the system is adapted to test a packaged memory device.

14. A method for testing a semiconductor memory device, said method comprising forcing the memory device into a logic state configuration not occurring during normal operation of the device.

15. The method as recited in claim 14, wherein said forcing comprises maintaining each of a pair of bitlines within the device at the same logic state, wherein the bitlines are complementary during normal operation of the device.

16. The method as recited in claim 15, wherein said maintaining comprises holding each of the bitlines at a circuit ground potential.

17. The method as recited in claim 14, wherein said forcing comprises using circuitry external to the memory device.

18. The method as recited in claim 15, wherein said forcing comprises flowing a direct current through the memory device from a voltage source to each of the pair of bitlines.

19. The method as recited in claim 18, wherein flowing a direct current through the memory device comprises flowing a direct current through at least one local interconnect structure of a bi-stable latch.

20. The method as recited in claim 14, wherein said forcing comprises holding the logic state configuration not occurring during normal operation of the device for a predetermined time.

21. The method as recited in claim 20, wherein said predetermined time is user-variable.

22. The method as recited in claim 14, said method further comprising performing a gross functional test on the memory device prior to said forcing.

23. The method as recited in claim 14, said method further comprising performing a gross functional test on the memory device after said forcing.

24. A method of stressing a semiconductor memory device comprising passing a first direct current through a first input node of a bi-stable latch within the memory device.

25. The method as recited in claim 24, wherein said passing the first direct current through the first input node comprises electrically coupling a first node within the memory device to a circuit ground potential and electrically coupling a second node within the memory device to a voltage source, wherein the first input node is arranged electrically between the first and second nodes.

26. The method as recited in claim 24, said method further comprising passing a second direct current through a second input node of a bi-stable latch within the memory device.

27. The method as recited in claim 26, wherein said passing the second direct current through the second input node comprises electrically coupling a third node within the memory device to a circuit ground potential and electrically coupling a fourth node within the memory device to a voltage source, wherein the second input node is arranged electrically between the third and fourth nodes.

28. The method as recited in claim 24, wherein the memory device comprises an SRAM.

29. The method as recited in claim 24, wherein said passing the direct current through the memory device occurs after packaging the device.